Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig.4. This sheet, which includes Figs. 4 and 5, replaces the original sheet including Figs. 4 and 5.

Attachment: Replacement Sheet

REMARKS/ARGUMENTS

Claims 14-22 have been amended. No claims have been canceled or added. Thus, claims 1-22 remain pending.

Claims 1, 9, 10, 12, 14 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Wallace (US PG Pub 2006/0117280), which is a continuation of U.S. Patent No. 7,020,855.

Claims 2-6, 11, and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace in view of Andreev et al. (6,848,094).

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace in view of Andreev et al. and in further view of Harrison et al. (5,636,368).

Claims 7, 8, 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace in view of Harrison et al.

Drawings

Figure 4 was objected to for non-uniform thickness of lines and for the non-conforming height of text. Figure 4 has been revised accordingly and a replacement sheet is enclosed. Accordingly, Applicants respectfully request withdrawal of this objection.

Rejection under 35 USC 112

Claims 14-22 are rejected under 35 USC § 112, ¶ 1, as failing to comply with the enablement requirement. Exemplary enablement, includes paragraph 83, which , e.g., states "processing unit 502 ... may execute a program stored in memory 504." Accordingly, Applicants respectfully request withdrawal of this rejection.

Claims 14-22 are rejected under 35 USC § 112, ¶ 2, as failing to set forth the subject matter which applicant regard as their invention. Applicant respectfully submits that as amended claims 14-22 satisfy 35 USC § 112, ¶ 2.

Rejection under 35 USC 102, Wallace

Claims 1, 9, 10, 12, 14 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Wallace (US PG Pub 2006/0117280), which is a continuation of U.S. Patent No. 7,020,855.

Claim 1 is allowable as Wallace does not disclose or suggest each and every element of claim 1. For example, claim 1 recites:

> *selecting first and second LUTs from the design;*
> *determining whether both of the LUTs implement a same function; and*
> *if the first and the second LUTs implement the same function, combining masks of the LUTs into a shared LUT mask in the design.*

Wallace is directed to a technique for finding input equivalences of a circuit so that the equivalent input pins may be swapped. *See Wallace '855*, column 1 lines 46-49. A circuit is decomposed into fanout-free regions and these regions are decomposed into netlists, which may include lookup tables as part of a circuit. *Id.,* Figures 4 and 5; col. 9 lines 12-23 and col. 15 lines 18-37. Once equivalent input pins are determined, "[s]uch pins can be swapped after placement and/or routing to reduce wire length, improve circuit timing, or reduce routing congestion." *Id.,* col. 3 lines 19-21. Thus, Wallace is concerned with optimizing routing resources.

Wallace describes circuits that implement the same logic function as being output equivalent. *Id.,* col.1 lines 35-41. However, Wallace is directed to finding input equivalence and not output equivalence. *Id.,* col. 1 lines 46-55 and col. 3 lines 38-40. ("Although techniques are provided for working with output equivalence, what are needed are techniques for identifying and exploiting input equivalences in the synthesis and layout of digital logic circuits.") This specific focus on input equivalence teaches away from Wallace being implemented for determining output equivalence.

Although Wallace does mention merging the functional forms of two adjacent AND gates into a larger AND gate, this does not teach or suggest combining masks of two LUTs as AND gates and LUTs are very different circuit elements. *Id.*, col. 9 lines 64-67. An AND gate has a single defined function, and thus there is no need to determine if two AND gates perform the same function. A LUT is programmable and could perform any function. Accordingly, Wallace does not teach or suggest determining if two circuits implement the same

function, and more specifically *"determining whether both of the LUTs implement a same function."*

Additionally, even if merging adjacent AND gates did suggest determining if LUTs implement a same function and combining them, Wallace provides no direction as to how the LUTs would be combined. Specifically, Wallace does not mention a mask of a LUT or any other type of mask, shared or otherwise. Thus, Wallace does not teach or suggest "*combining masks of the LUTs into a shared LUT mask in the design*" as recited in claim 1.

For at least the reasons given, Applicant submits that claim 1 and its dependent claims 2-13 are allowable over Wallace. Applicants submit that independent claim 14 should be allowable for at least the same reasons as claim 1. Claims 15-22 depend from claim 14 and thus derive patentability at least therefrom.

Rejection under 35 USC 102, Wallace in view of Andreev

Claims 2-6, 11, and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace in view of Andreev.

Claims 2-6 and 11 depend upon claim 1 and are allowable for at least the same rationale as claim 1. Claims 15-19 depends upon claim 14 and are allowable for at least the same rationale as claim 14. Andreev does not make up for the deficiencies in these claims with respect to Wallace. For example, Andreev does not mention a LUT, and redundant nets are removed (in step 712) and not combined into "*into a shared LUT mask*". *See Andreev*, Figure 7; col. 7 lines 18-24.

These claims are also allowable for additional reasons. For example, Andreev does not teach or suggest rearranging input signals to the input terminals of a LUT and determining if both LUTs implement the same function based on the rearrangement, as recited in these claims.

In Andreev, a variable set representative of the inputs and outputs of logic elements in the netlist is generated. *See Andreev*, abstract. "In step 708, the variable set is re-ordered so that the inputs of the logic elements are ordered before the outputs. For example, if a logic element has inputs a and b and an output c, then the inputs a and b are ordered before the output c." *Id.*, Figure 7 and col. 7 lines 7-10. Thus, the rearranging involves the order of the

inputs of one logic element and the output of that logic element within the variable set. Accordingly, the input signals are not rearranged either to the input terminals of the logic elements or even in the variable set.

Furthermore, Andreev determines an equivalent function based whether a key has the same inputs and the same output function table. *Id.*, col. 3 lines 31-33. If the key is not found, then a new entry is provided and the logic functions are determined to be not equal. *Id.*, col. 3 lines 33-36. Thus, there is no further determination if the logic elements are equal after a rearrangement. For at least these additional reasons, Applicant submits that claims 2-6, 11, and 15-19 are allowable over Wallace in view of Andreev.

Rejection under 35 USC 102, Wallace in view of Harrison

Claims 7, 8,13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace in view of Harrison.

Claims 7, 8, and 13 depend upon claim 1 and are allowable for at least the same rationale as claim 1. Claim 20 depends upon claim 14 and is allowable for at least the same rationale as claim 14. Harrison does not make up for the deficiencies in these claims with respect to Wallace and Andreev. Harrison is directed to mapping a function onto one of multiple function block types based on the properties of the function. *See Harrison*, col. 2 lines 38-40. Harrison does not mention a LUT, determining if LUTs implement the same function, or combining LUTs in the same mask.

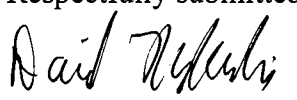
These claims are also allowable for additional reasons. For example, Harrison does not teach or suggesting determining the number of common or non-common inputs between two functions, let alone two LUTs. At step 820, it is determined whether a single function has a sufficient number of inputs. *Id.*, col. 11 lines 37-41. If the single function has too many inputs, it may be split into subfunctions. *Id.*, col. 11 lines 65-67. Harrison does not mention comparing common inputs to two functions, and functions are not prevented from being combined as there is no combining in the first place. Thus, Harrison does not teach or suggest determining the number of common or non-common inputs of two LUTs or preventing the masks from being combined, as recited in these claims. For at least these additional reasons, Applicant submits that claims 7, 8,13 and 20 are allowable over Wallace and Andreev in view of Harrison.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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Attachments
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